Analog frequency divider by variable order 6 to 9

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Abstract — **In this work, concepts from nonlinear dynamics are applied for the design of analog frequency dividers of variable order. The design takes advantage of the multiple Arnold tongues of highly nonlinear oscillators. The variation in the division order is obtained through the modification of a circuit parameter, like, for instance, the capacitance of a varactor diode. Here the design of a bipolar-based analog frequency divider, whose division order can be 6, 7, 8 or 9, is presented. A new simulation tool is proposed for the harmonic-balance analysis of high-order divisions. The circuit has been manufactured and experimentally characterized, with excellent results.**

I. INTRODUCTION

Bifurcation theory offers unexplored possibilities to obtain operation modes and analog functions that cannot be implemented from standard design concepts. In particular this paper presents the design of an analog frequency divider of variable order 6 to 9. The advantage of this analog division is the possibility of implementation at high microwave frequencies.

When connecting an input generator to a free-running oscillator, synchronization bands are theoretically formed at all the rational ratios between the self-oscillation frequency ω_o and the input generator frequency ω_{in}, i.e., ω_o/ω_{in}=M/N [1]. The width of the synchronization bands increases with the input power P_{in}, giving rise, in the plane defined by ω_{in} and P_{in}, to tongue-shaped curves (one for each M/N), delimiting the region of synchronized behavior. These curves are called Arnold tongues [1]. Their width usually decreases fast with M and N.

In general, outside the synchronization bands, there is a regime with two incommensurate fundamentals or quasi-periodic regime. Thus, as ω_{in} is modified (system parameter), periodic and quasi-periodic intervals alternate. In other cases, the operation regime between the periodic intervals (also called windows) is chaotic, this giving rise, as the parameter evolves, to what is called a period-adding route to chaos [1]. In this case, periodic and chaotic intervals alternate versus the parameter (ω_{in}).

The synchronization bands are delimited (at each end) by bifurcations of saddle-node type [1-2]. When tracing the periodic solution curve (in terms of output power, for instance) versus a suitable parameter, such as ω_{in}, the saddle-node bifurcations give rise to turning points (infinite-slope points) [3]. Thus, synchronization curves are typically closed.

The natural formation of Arnold tongues (M/N) in injected oscillators should allow divisions of any order. To obtain wide Arnold-tongues, a careful nonlinear design must be carried out. The objective here is the widening of periodic windows of large division order 1/N. Another objective is to be able to change the division order of the divider circuit, for a given input-frequency band ω_{in1}, ω_{in2}. Advantage can be taken of the fact that bifurcation patterns, versus different parameters of the same system, are often similar. This should enable varying the division order versus a suitable parameter, such as a varactor voltage. Two parameters will be considered in the analysis: the input frequency ω_{in}, to ensure a certain operation band, and an additional parameter, to change the division order. The latter could be the capacitance of a varactor diode.

The Poincaré map technique [3] enables a simple determination of periodic windows, but is only applicable to circuits that can be simulated in time domain. In addition, even when applicable, simulations are usually unbearable long. This limits the use of the tool to circuit analysis, rather than actual design. On the other hand, harmonic balance (HB) is efficient for frequency divisions of low order, but usually lacks accuracy for divisions of high order. In previous works, cascades of frequency divisions by two have been analyzed through HB [4]. To our knowledge, it has never been employed to obtain high-order divisions by synchronization. The development of efficient simulation tools for this kind of behavior has been another objective here.

A variable order divider, based on a bipolar transistor, has been manufactured and experimentally characterized. However, the aim is not to present an ultimate design, but to show the possibility of using principles and knowledge from bifurcation theory to obtain specific circuit performance.

II. CIRCUIT DESIGN AND OPERATION

In the design of the variable-order frequency divider, a relatively low input frequency f_{in}≅2 GHz, has been chosen, to facilitate the use of time-domain tools (in addition to frequency-domain analysis and measurements). The first

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stage to obtain an analog divider is the design of a free-running oscillator. Here the self-oscillation frequency was $f_o \cong 0.2$ GHz, to enable high order divisions. In order to have wide Arnold-tongues (or synchronization bands 1/N), the free-running oscillation must be very nonlinear, with high harmonic content. In this design, the active element is a bipolar transistor. The circuit topology is similar to that of a classical Colpitt's oscillator (Fig. 1). The principles of the design are, however, very general, and could be applied to other active devices and circuit topologies.

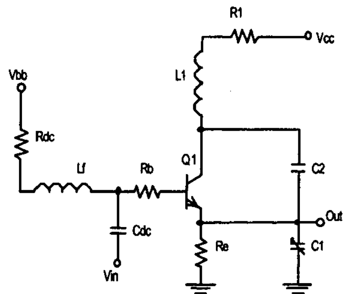

Fig. 1. Schematic of the variable-order frequency divider.

The bipolar transistor is biased near cut-off. The values of the active elements are selected so as to increase the nonlinearity of the limit cycle (Fig. 2). The transistor is in cut-off for about half of the oscillation period, which gives rise to high harmonic content. The input signal of the divider is introduced through the base terminal and the output signal is extracted at the emitter terminal. The output extraction through a buffer amplifier at the collector terminal is also possible.

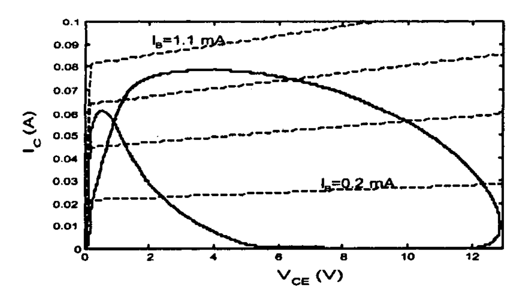

Fig. 2. Limit cycle of the free-running oscillation.

In the presence of a sinusoidal generator of frequency ω_{in}, the synchronization of a given harmonic component $N\omega_o$ to the input signal gives rise to a division by N. This synchronization is more easily obtained for higher amplitude of the harmonic term $N\omega_o$. A larger synchronization bandwidth can also be expected for higher harmonic amplitude.

II. CIRCUIT ANALYSIS

A. Analysis through the Poincaré map.

The synchronization bands, in terms of a given parameter, can be determined through time-domain integration by using the technique of the Poincaré map. In this technique, once the steady state has been reached, samples are taken at integer multiples of the input generator period nT_{in}. If the solution has the same period as the input generator, a single point is obtained. If the period of the solution is a multiple of that of the input generator period NT_{in}, N different points are obtained. This analysis has been carried out in Fig. 3, where samples of the collector current I_c are traced versus the capacitance C_1, for constant input voltage V_{in} = 0.5 v and f_{in}=1.9 GHz. According to the capacitance value, divisions by N = 6 to N = 12 can be obtained. The capacitance interval for each division order is about 2 pF. Thus, the use of a varactor diode should enable a simple variation of the division order.

For this input voltage value (V_{in} = 0.5 v), there are narrow intervals of chaotic behavior, between the frequency-division windows. The chaotic solutions appear at the saddle-node bifurcations (delimiting the synchronization bands), through an intermittency process [2]. The chaotic intervals are relatively narrow and, as the input voltage increases, become negligible small, for some division transitions. For lower input voltage, the behavior between the periodic windows is quasi-periodic.

Two are the drawbacks of the Poincaré map technique when analyzing microwave dividers: on the one hand, not all the circuits can be simulated in time domain. On the other hand, the computation time is too high.

B. Analysis through harmonic balance

When employing frequency-domain techniques for the analysis of high-order divisions, accuracy problems may arise, due to the high-harmonic value of the input generator, with respect to the free-running oscillation. Another problem comes from the fact that each region of periodic behavior is bounded by two saddle-node bifurcations, giving rise to turning points of the synchronization curve.

In [2-4], the division curves are obtained by introducing an auxiliary generator (AG) into the circuit. When using a voltage AG, it is connected in parallel at a circuit node, close to the transistor terminals. The AG must fulfill a non-perturbation condition of the steady state (given by a zero value of its associated admittance Y_T). For the analysis of a possible division by N, the frequency of the generator is fixed to $\omega_{AG}=\omega_{in}/N$. In [2-4], for each value of the analysis parameter, the AG amplitude A_{AG} and phase ϕ_{AG} are either optimized or calculated (through an error-minimization algorithm) to fulfill Y_T=0. This procedure, based on the optimization/calculation of the AG amplitude and phase, does not seem to provide good convergence results for divisions of high order.

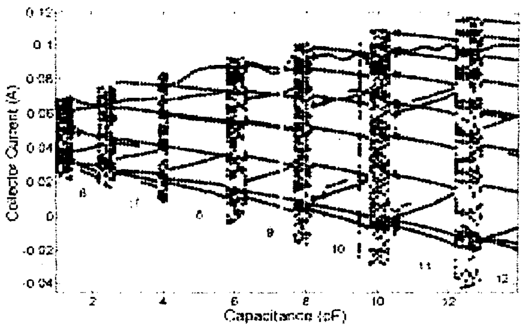

Fig. 3. Poincaré map of the frequency divider, Collector current I_C versus the capacitance C_1.

The new procedure is the following. An initial optimization is carried out, in the three variables ω_{in}, A_{AG} and ϕ_{AG}, to fulfill Y_T=0. From the resulting point ω_{ino}, A_{AGo} and ϕ_{AGo}, a sweep is carried out in the AG phase ϕ_{AG}, between ϕ_{AGo} and $\phi_{AGo} + 2\pi/N$. For each point of the sweep, the two variables A_{AG} and the parameter (in this case, either ω_{in} or C_l) are optimized or determined (through a suitable error-minimization algorithm), in order to fulfill Y_T=0. This technique is illustrated in Fig. 4, obtaining the division band 1/8 versus C_l. Each solution point of the phase sweep (Fig. 4b) is a point of the closed synchronization curve (Fig.4a).

Note that the circuit variables and the parameter are periodic in phase (Fig. 4b) and do not exhibit turning points versus this variable, which enables a straightforward tracing of the synchronization curve. The outer turning points delimit the synchronization band. A complementary stability analysis is necessary to determine the stable solution section. In this case, the upper part of the curve (between the two outer turning points) is stable. The synchronization bandwidth is given by the absolute minimum and maximum of the curve C_l (ϕ_{AG}), i.e, $dC_l/d\phi_{AG}=0$ (see Fig. 4b). This enables a simple numerical technique for tracing the synchronization loci. Note that, in the design, the purpose will be to increase the size of the synchronization curves and this simulation technique enables fast design tuning. In Fig. 5, two synchronization curves are traced, through the frequency-domain, technique, versus C_1. For the sake of clarity of the representation, only two curves have been included, corresponding to the division orders N=7 and N=8. In each case, the upper half of the closed curve is stable. All the circuit parasitics have been taken into account. The good agreement with Fig. 3 is evidenced. The increase in the output power with the division order comes from the associated reduction of the divided frequency. Two measurement points have been superimposed. In the evaluation of this first prototype, different capacitances have been used.

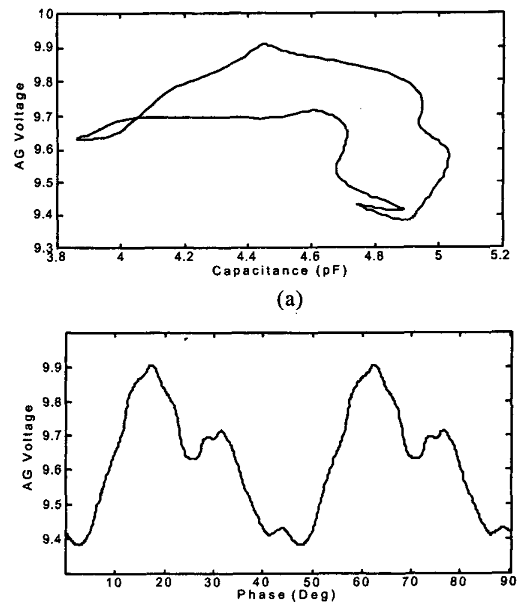

Fig. 4. New technique for obtaining the closed synchronization curves, through phase sweep. Maxima and minima determine the synchronization band and the jump points.

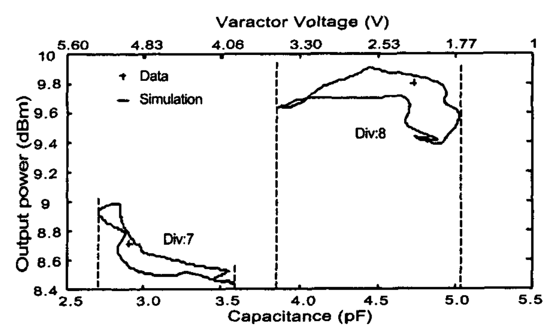

Fig. 5. Synchronization bands in frequency domain.

To determine the synchronization bandwidths in terms of the input frequency, the corresponding Arnold tongues are traced in Fig, 6. The capacitance is now fixed to C_l=4.7 pF. The influence of the base resistance has been studied.

The lower the value of this resistance, the larger the synchronization bandwidth. Measurement points for R=62 Ohm also included, for division order 7 to 9. In fact, frequency-division bands with order N=2 to N=12 have experimentally been observed.

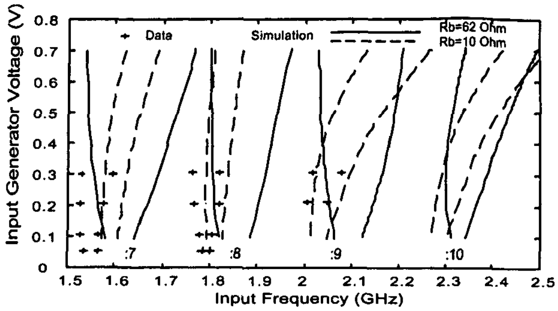

Fig. 6. Arnold tongues versus input frequency for two values of the base resistor.

IV. EXPERIMENTAL OUTPUT SPECTRUM

The output spectrum of the variable-order divider, for two different values of the capacitance C_1, is shown in Fig. 7. In both cases, the input frequency is fixed to f_{in}=1.534 GHz. As observed, the initially free-running oscillator has a rich harmonic content. Fig. 7a shows the typical triangular spectrum about the eighth harmonic component, proving the actual synchronization phenomenon. In Fig. 7b, a division by N=7 has taken place. In Fig. 7c, the division order is N=8. In agreement with the simulations, the variation of the capacitance gives rise to a modification of the division order. The measured phase noise of the divided frequency component is, in both cases, about −70 dBc/Hz at 1 KHz offset. This divided component must be selected through proper filtering at the circuit output. The measurements of the synchronization bandwidth versus the input frequency have been superimposed in former figures

V. CONCLUSION

The design of an analog frequency divider with variable division order has been presented. The design of the divider relies on the multiple Arnold tongues of highly nonlinear oscillators. The circuit is analyzed through the Poincaré map and through the phase sweeps of an auxiliary generator. The latter technique enables fast design tuning. The modification of the division order is achieved through variation of a circuit capacitance. A frequency divider with variable order N=6 to N=9 has been designed and experimentally characterized, with excellent results.

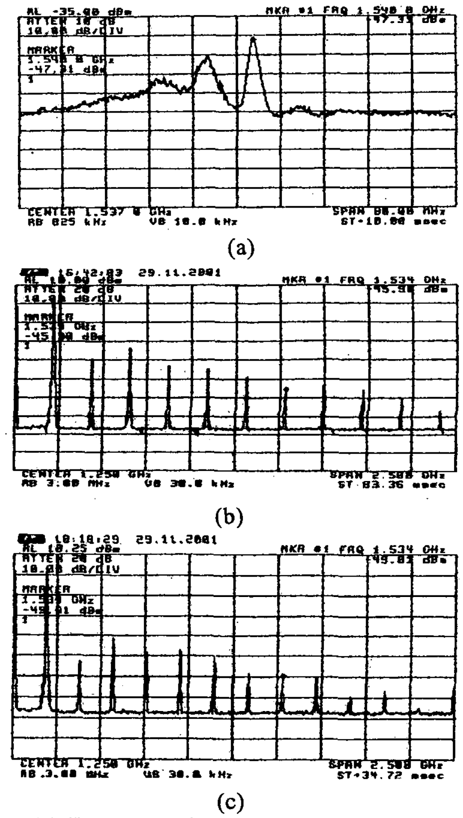

Fig. 7. (a) Triangular shape of the near-synchronization spectrum. (b) Division by 7, f_{in}=1.534 GHz (C_1=2.9 pF). (b) Division by 8, f_{in} 1.534 GHz (C_1=4.7 pF).

ACKNOWLEDGEMENT

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